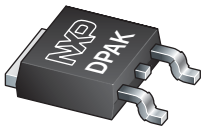


ACTT4S-800C

AC Thyristor Triac power switch

Rev. 1 — 29 March 2012 Product data sheet

1. Product profile

1.1 General description

Planar passivated AC Thyristor Triac power switch in a SOT428 (DPAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients.

1.2 Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Less sensitive gate for high noise immunity
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Sensitive gate for easy logic level triggering
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

1.3 Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; see Figure 5; see Figure 6	-	-	35	A
T_j	junction temperature		-	-	125	°C

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 108$ °C; see Figure 1; see Figure 2; see Figure 4	-	-	4	A
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; see Figure 3	-	-	2	kV
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; see Figure 8	-	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; see Figure 8	-	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; see Figure 8	-	-	35	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C	850	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; see Figure 13	1000	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit; see Figure 14; see Figure 15	8	-	-	A/ms

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	mb	LD
2	LD	load		G
3	G	gate		
mb	LD	mounting base; load	2	CM
			1 3	003aaf29(
			SOT428 (DPAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT4S-800C	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 108$ °C; see Figure 1; see Figure 2; see Figure 4	-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; see Figure 5; see Figure 6	-	35	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms	-	39	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse	-	6	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs	-	100	A/µs
I_{GM}	peak gate current	t = 20 µs	-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C
V_{PP}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; see Figure 3	-	2	kV

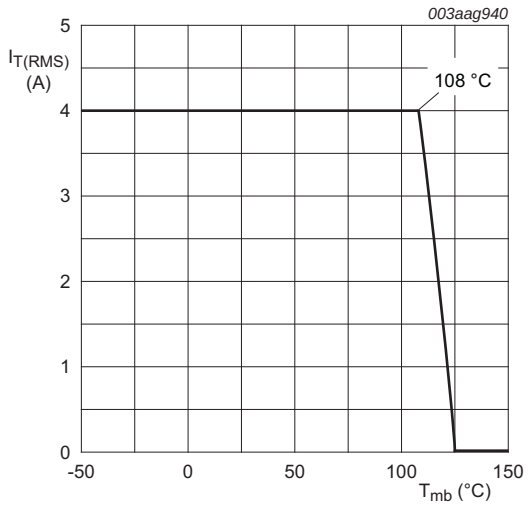
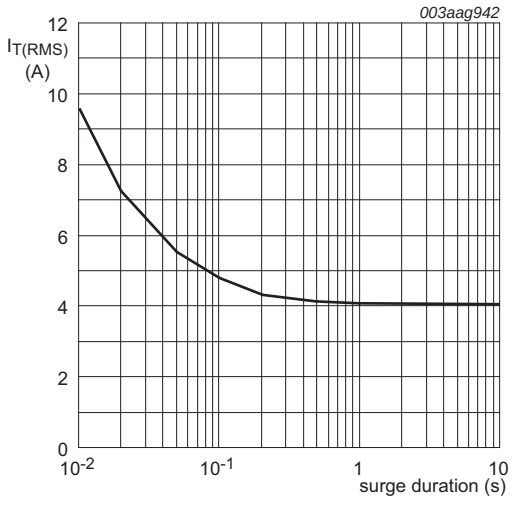


Fig 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz; T_{mb} = 108 °C

Fig 2. RMS on-state current as a function of surge duration; maximum values

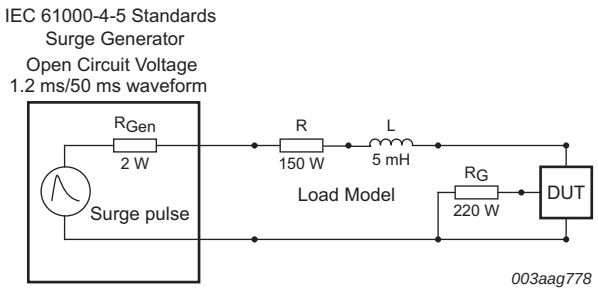
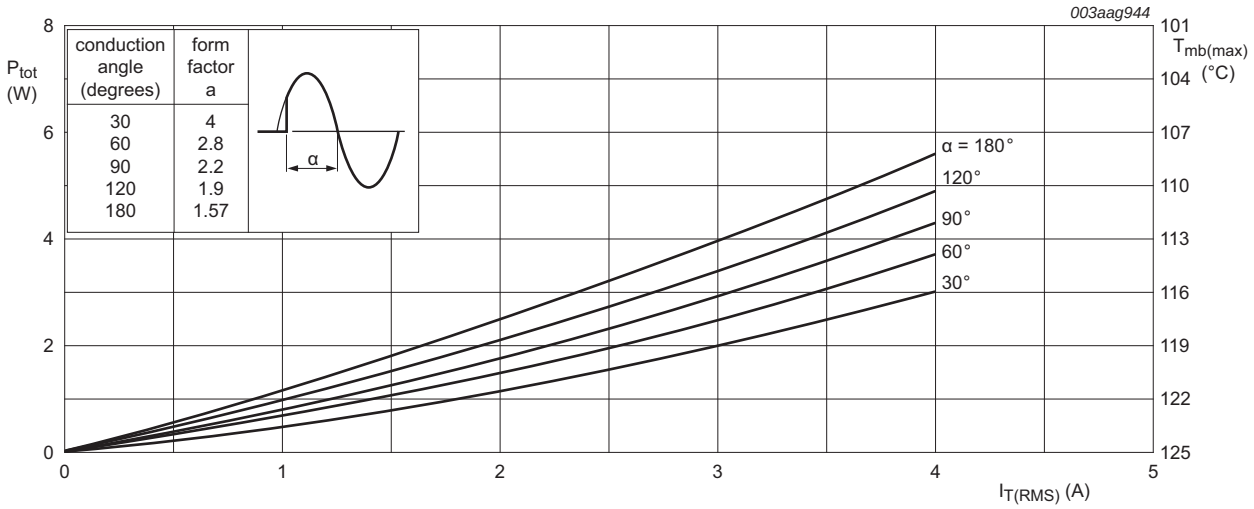


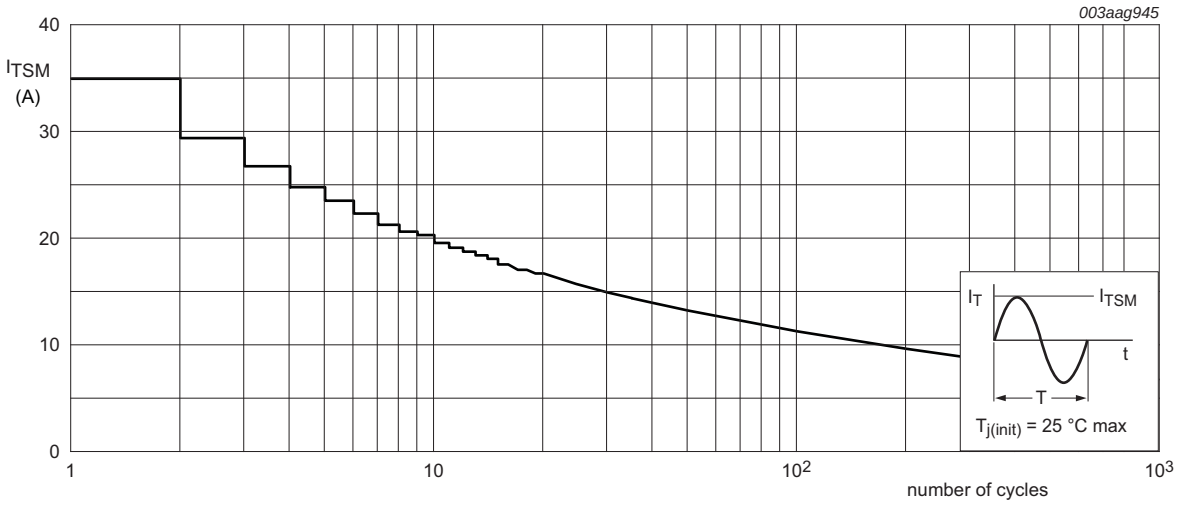
Fig 3. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5



α = conduction angle

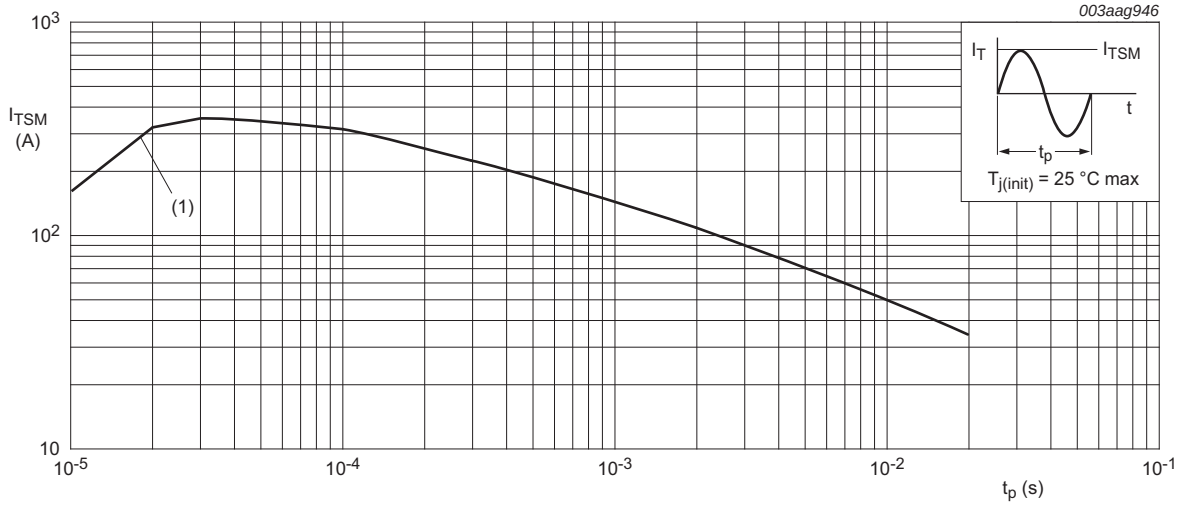
a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig 4. power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



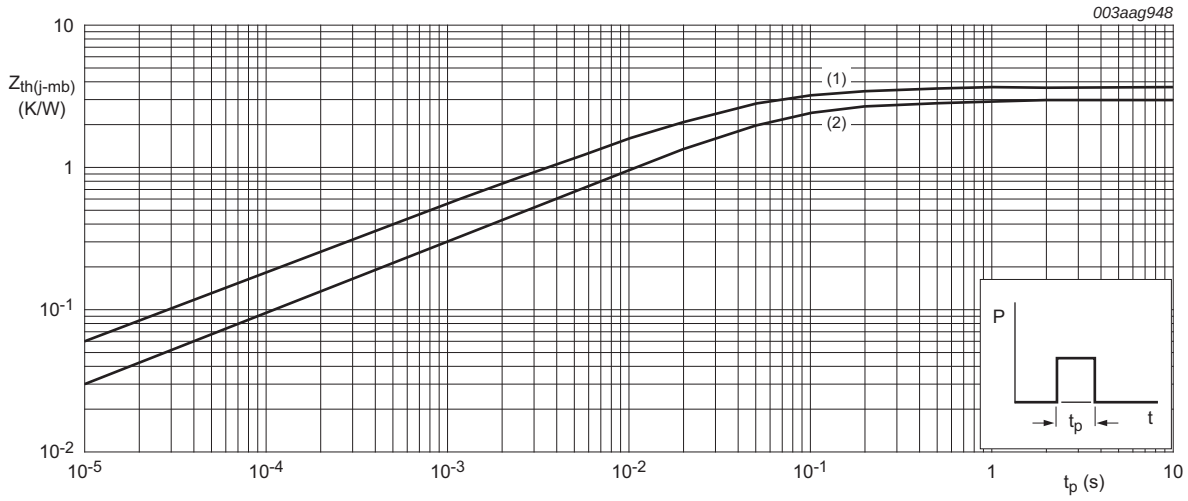
$t_p \leq 20$ ms; (1) dI_T / dt limit

Fig 6. Non-repetitive peak on-state current as a function of pulse width; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; see Figure 7	-	-	3	K/W
		half cycle; see Figure 7	-	-	3.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	75	-	K/W



(1) Unidirectional (half cycle)

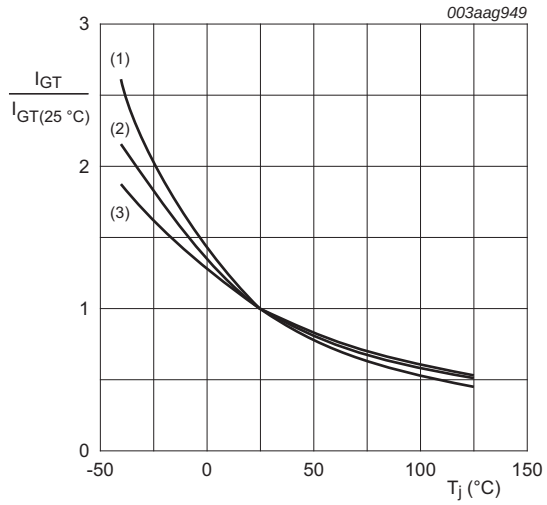
(2) Bidirectional (full cycle)

Fig 7. Transient thermal impedance from junction to mounting base as a function of pulse width

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; see Figure 8	-	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; see Figure 8	-	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; see Figure 8	-	-	35	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G+; T_j = 25 °C; see Figure 9	-	-	50	mA
		V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; see Figure 9	-	-	60	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; see Figure 9	-	-	50	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; see Figure 10	-	-	35	mA
V_T	on-state voltage	I_T = 6 A; T_j = 25 °C; see Figure 11	-	-	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 100 mA; T_j = 25 °C; see Figure 12	-	-	1.5	V
		V_D = 400 V; I_T = 100 mA; T_j = 125 °C; see Figure 12	0.2	-	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C	-	-	10	µA
		V_D = 800 V; T_j = 125 °C	-	-	0.5	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C	850	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; see Figure 13	1000	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit; see Figure 14; see Figure 15	8	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 10 V/µs; gate open circuit; see Figure 14; see Figure 15	10	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 1 V/µs; gate open circuit; see Figure 14; see Figure 15	15	-	-	A/ms



(1) LD- G-

(2) LD+ G+

(3) LD+ G-

Fig 8. Normalized gate trigger current as a function of junction temperature

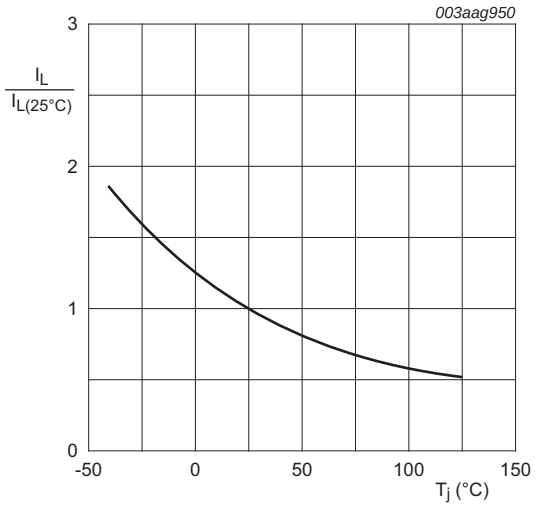


Fig 9. Normalized latching current as a function of junction temperature

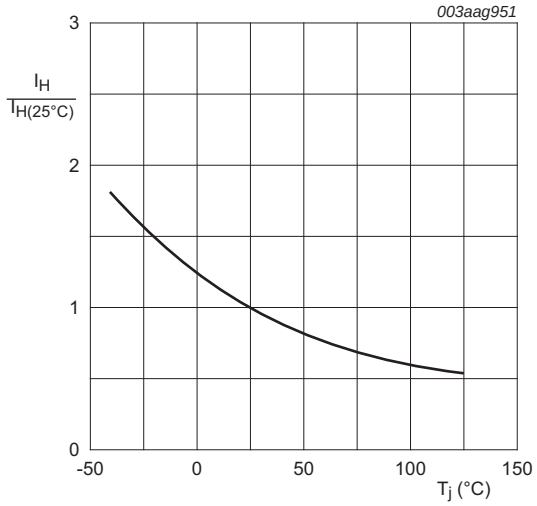
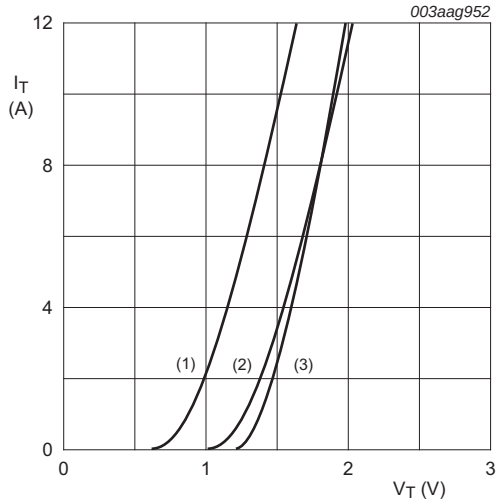


Fig 10. Normalized holding current as a function of junction temperature



V_o = 1.242 V; R_s = 0.074 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig 11. On-state current as a function of on-state voltage

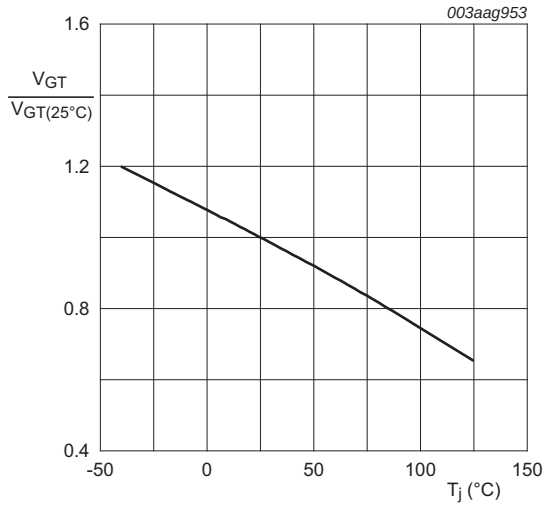
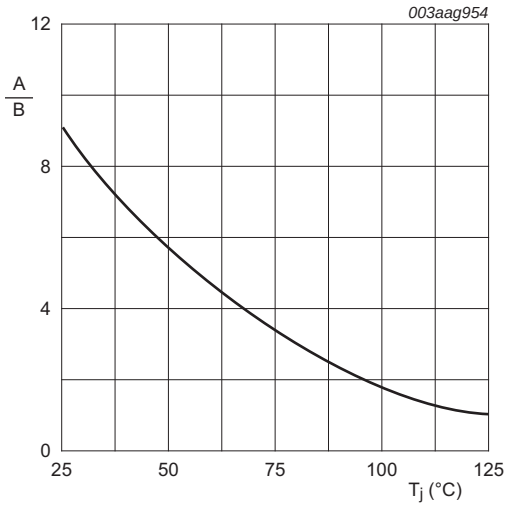


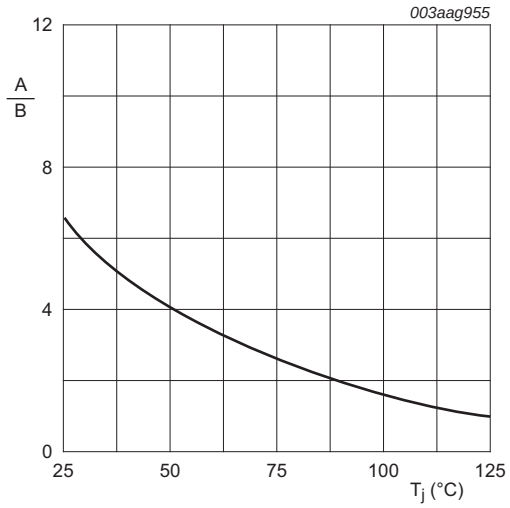
Fig 12. Normalized gate trigger voltage as a function of junction temperature



A is dV_D/dt at condition T_j °C

B is dV_D/dt at condition T_j 125 °C

Fig 13. Normalized rate of rise of off-state voltage as a function of junction temperature

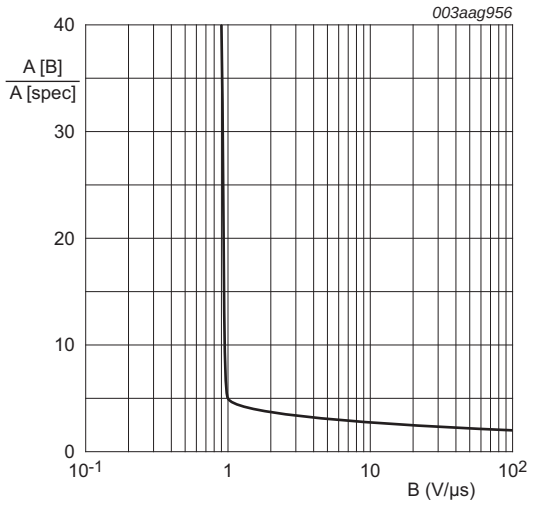


A is dI_{com}/dt at condition T_j °C

B is dI_{com}/dt at condition T_j 125 °C

V_D = 400 V

Fig 14. Normalized critical rate of rise of commutating current as a function of junction temperature



A[B] is dI_{com}/dt at condition B, dV_{com}/dt

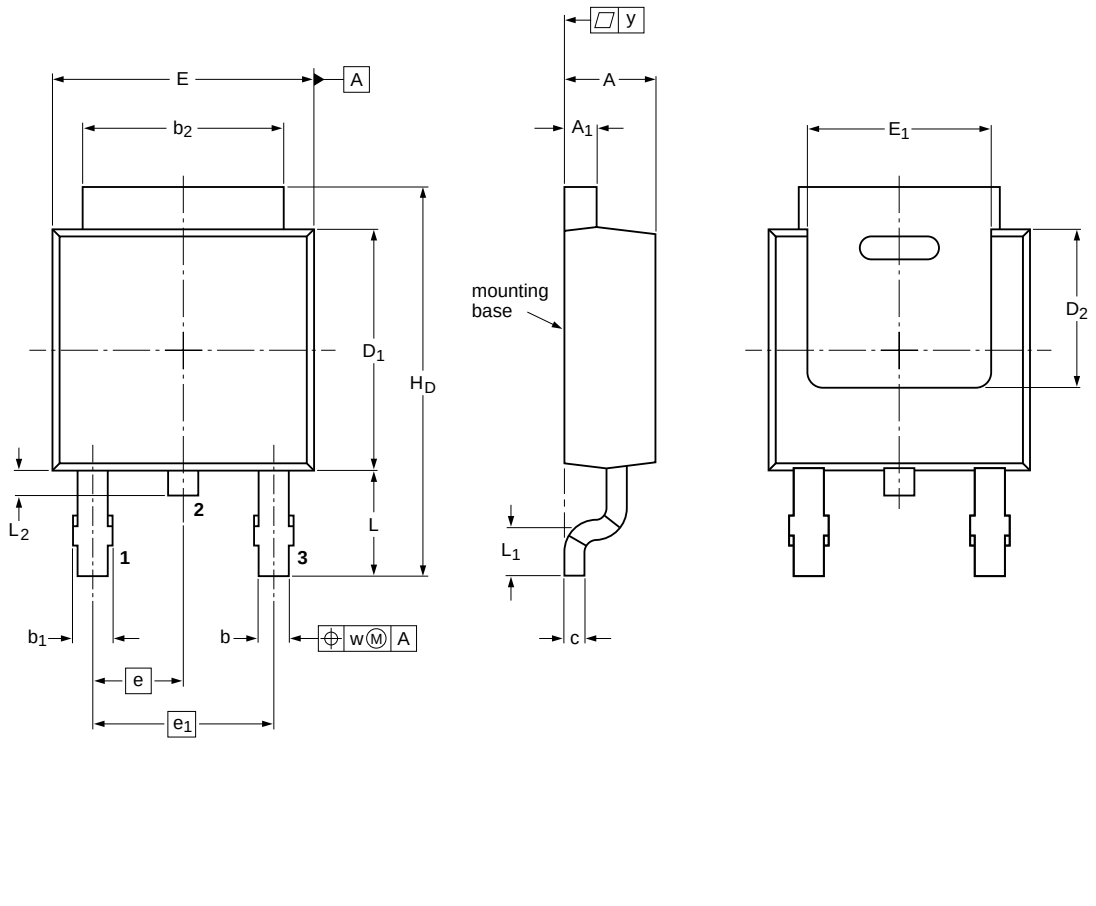
A[spec] is the specified data sheet value of dI_{com}/dt

turn-off time < 20 ms

Fig 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 16. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ACTT4S-800C v.1	20120329	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URLhttp://www.nxp.com.

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For more information, please visit:http://www.nxp.com

For sales office addresses, please send an email to:salesaddresses@nxp.com

11. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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